Abstract of the Disclosure

Provided is a method of manufacturing a semiconductor device having a first region, in which a capacitance component is a dominant cause of a RC delay, and a second region, in which a resistance component is a dominant cause of a RC delay. The method comprises performing a first etching process to an insulating layer formed on a semiconductor substrate, so that a first trench having a first thickness and a second trench having the first thickness are formed in the first region and the second region, respectively; performing a second etching process to the second trench, so that a third trench having a second thickness thicker than the first thickness is formed in the second region; filling the first trench and the third trench with a metal layer; and removing portions of the metal layer, so that a first metal interconnection and a second metal interconnection are formed inside of the first trench and the third trench, respectively.

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